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# 1 [Interactive global illumination in dynamic scenes](#)

Parag Tole, Fabio Pellacini, Bruce Walter, Donald P. Greenberg

 July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual**
**conference on Computer graphics and interactive techniques**, Volume 21 Issue 3

 Full text available: [pdf\(13.82 MB\)](#)

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In this paper, we present a system for interactive computation of global illumination in dynamic scenes. Our system uses a novel scheme for caching the results of a high quality pixel-based renderer such as a bidirectional path tracer. The Shading Cache is an object-space hierarchical subdivision mesh with lazily computed shading values at its vertices. A high frame rate display is generated from the Shading Cache using hardware-based interpolation and texture mapping. An image space sampling sc ...

**Keywords:** Monte Carlo techniques, illumination, parallel computing, ray tracing, rendering, rendering systems

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## Handshake-wave combined approach with runtime reconfiguration for designing a low latency asynchronous FIFO

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### Abstract

In this paper, a novel design scheme combining a handshake protocol and wave pipeline is proposed to improve latency performance of an asynchronous linear FIFO. The stage control of the proposed FIFO can be reconfigured dynamically to be one of two different operating styles, waving or handshaking according to the status of data flow in the FIFO. The use of wave pipelining in a control and a datapath can eliminate delays of handshaking circuits and latching data respectively. The proposed circuits have been designed with 0.25  $\mu\text{m}$ , 2.5 V CMOS process technology and simulated using HSPICE. Preliminary results show about two times improvement on latency performance over a state-of-art linear FIFO circuit while retaining throughput and a simple linear structure.

### Index Terms

#### Inspec

##### Controlled Indexing

CMOS logic circuits SPICE asynchronous circuits flip-flops logic CAD pipeline processing

##### Non-controlled Indexing

CMOS process technology FIFO design HSPICE asynchronous linear FIFO baseline control structure handshake-wave combined approach latch control latency performance low latency asynchronous FIFO runtime reconfiguration stage control wave pipelining

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